Design of an analog defuzzifier in CMOS tecnology

Projeto de um defuzificador alalogico em tecnologia CMOS

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Abstract

The use of intelligent controllers applied to industrial systems has been getting usual, not only in the process control as in the literature. The most utilized control methodology, within the artificial intelligent techniques, is based in fuzzy logic. Fuzzy logic controllers consist of the following modules: fuzzification, decision making and defuzzification. Various defuzzification circuits architecture have been proposed in the literature. The efficacy of a fuzzy logic controller depends very much on defuzzification process. This paper aims to present the project for an analog defuzzifier circuit operating in current-mode to be implemented in CMOS 0.35? AMS. From the hardware point of view, the main characteristics of the proposed defuzzifier circuit are simplified architecture, small chip area and low power-supply voltage. The simulation result of each defuzzifier circuit block will be presented: scaling, addition and division. And also, the output current graphic of the complete circuit, compared with theoretical values. All simulation results have been obtained by the use of SPICE software. The proposed circuit in this work is part of a general-purpose fuzzy microprocessor, and can be applied to many control systems, as for example the control of a DC motor

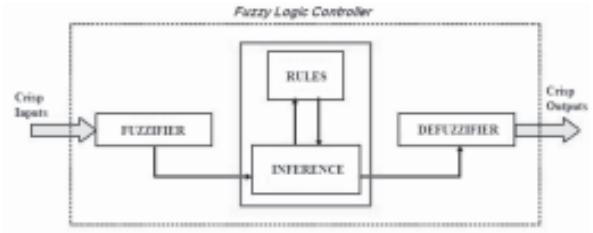
Keywords

Defuzzifier, Fuzzy controller, Microprocessor, Fuzzy Hardware

1. Introduction

Over several past years, fuzzy systems have been successfully applied to a wide range of practical problems. Therefore, researchers have been studying new architectures of fuzzy logic systems towards the improvement performance of these circuits. Various architectures of fuzzy logic controller have been proposed in the literature (Bouras et al., 1998 - Guo et al., 1996 - Yamakawa, 1986), with the purpose to help engineers to implement complex and ill-defined control systems.

A fuzzy logic controller has the following components: fuzzifier, inference engine and defuzzifier, as shown in Fig. 1 (El, 1998 - Mendel, 1993).



igure 1- Fuzzy Logic Controller blocks diagram.

The fuzzifier maps crisp numbers into fuzzy sets. The inference engine is the main block of the fuzzy logic controller. It handles the way in which rules are combined; this block stores the rules of the knowledge base that is used by the processor to solve a problem. The defuzzifier maps output fuzzy sets into crisp numbers. There are several architectures of defuzzifier circuits in the literature (Huertas, et al., 1996 - Miki, 1997 - Baturone, et all, 1997 - Tang and Lin, 1995 - Tsukano,1995). In this paper we propose an analogue current-mode defuzzifier circuit, based on Height strategy.

This paper was divided in the following sections: section 2 presents the defuzzifier circuit architecture and one detailed description of all constituent blocks

of this circuit, section 3 presents the result of simulation of the circuit designed, and finally in section 4 the conclusion of the work are presented.

Resumo

O uso de controladores inteligentes aplicados a sistemas industriais está sendo utilizado tanto no controle de processos industriais como na literatura especializada. Entre as técnicas de Inteligência Artificial, as metodologias de controle mais utilizadas são baseadas na Lógica Difusa. O controlador baseado na Lógica Difusa consiste dos seguintes módulos: Fuzificação, Inferência e Defuzificação. Varias arquiteturas de circuitos defuzificadores foram propostas na literatura. A eficácia do controlador baseado em lógica difusa depende muito dom processo de defuzificação. O objetivo deste artigo é apresentar o projeto de um defuzificador analógico, que opera em modo corrente na tecnologia CMOS 0,35 da AMS. Do ponto de vista de hardware, as principais características do circuito defuzificador proposto são: arquitetura simplificada, utilização de pequena área de silício e baixa potência. O resultado de simulação de cada bloco do circuito defuzificador será apresentado: escalonador, somador e divisor. E também, o gráfico da corrente de saída do circuito completo, comparado com os valores teóricos. Todos os resultados de simulação foram obtidos utilizando o software SPICE. O circuito proposto neste trabalho é parte de um microprocessador baseado em lógica difusa de propósito geral, e pode ser aplicado a muitos sistemas de controle, como por exemplo, o controle de um motor DC.

Palavras-Chave

Defuzificador. Controlador difuso. Microprocessador analógico. Hardware analógico.

2. Proposed architecture

The architecture of the defuzzifier circuit proposed in this paper is based on Height defuzzification strategy, the general expression of this strategy can be written as:

$$w^* = \frac{\sum_{i=1}^{m} h_i \cdot c_i}{\sum_{i=1}^{m} h_i} \qquad (1)$$

where c_i is the peak value position of membership function, h_i is the activation degree of each rule (height) and m the number of membership functions.

The proposed defuzzifier circuit will be used as part of a two input one output fuzzy logic controller, with five membership functions. Then, the Equation (1) can be written as:

$$w^* = \frac{h_1 \cdot c_1 + h_2 \cdot c_2 + h_3 \cdot c_3 + h_4 \cdot c_4 + h_5 \cdot c_5}{h_1 + h_2 + h_3 + h_4 + h_5} \qquad (2)$$

To implement an architecture based on Equation (2), it would be necessary five multiplier circuits, two adders and one divider. In the proposed architecture, the position values of the membership function were defined: c_1=5µA, c_2=10µA, c_3= 15µA, c_4= 20µA e c_5=25µA. Substituting theses values in the Equation (2), then:

$$w^* = \frac{5\mu \cdot (h_1 + h_2 \cdot 2 + h_3 \cdot 3 + h_4 \cdot 4 + h_5 \cdot 5)}{h_1 + h_2 + h_3 + h_4 + h_5} = \frac{5\mu \cdot \sum f^*}{\sum f} = \frac{c_1 \cdot \sum f^*}{\sum f} \qquad (3)$$

The Figure 2 shows the architecture based in Equation (3). This architecture is composed of a three level structure, the first level is composed by scalers circuits, followed by adders circuits and the third level is composed by a multiplier-divider circuit. In this architecture the multiplier operation is implemented by scalers circuits, compared to analog multiplier circuit it is easier to implement and uses small number of transistors. It takes advantage of analogue approach such as high speed and small chip area; it also has advantages of low power-supply voltage.

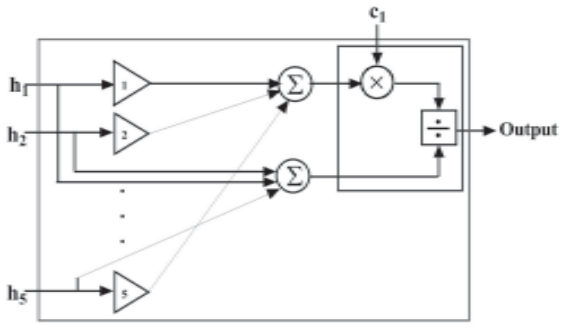


Figure 2- Defuzzifier architecture for height strategy.

2.1 Scaler Circuit

The scaler circuit multiplies the activation degree of the rules (h_1, h_2, h_3, h_4 e h_5) by the position of membership functions (1, 2, 3, 4, 5).

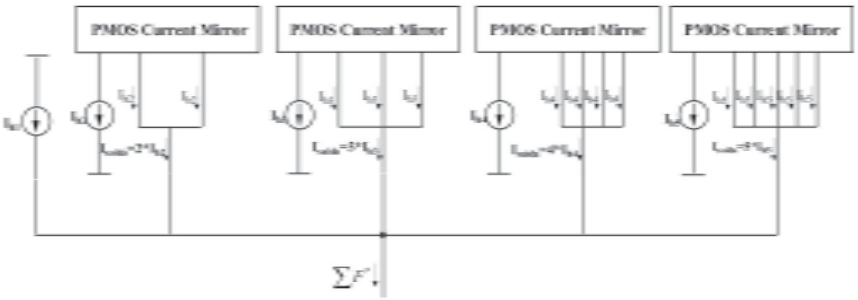


Figure 3- Entire Scaler circuit block diagram.

The circuit is composed of type P CMOS transistors with same dimensions that are connected as cascade current mirror with ratio stated in 1:1, 1:2, 1:3, 1:4 and 1:5 , as shown in Fig. 3. It was projected to consume low power and small chip area.

The scaler circuit h5 based on cascode current mirror is shown in Fig. 4. In CMOS current mirror design the best matching is achieved by using identical, multiple devices conected in parallel (Allen, 2002).

2.2 Adder Circuit

The adder circuit is required to obtain the numerator ($\sum f^*$) and denominator ($\sum f$) of the defuzzifier circuit architecture of the Fig. 2.

One of the advantages of current-mode techniques was exploited to implement this circuit, so based on the current Kirchhoff's law, currents can be added by simply connecting wires, as shown in Fig. 5.

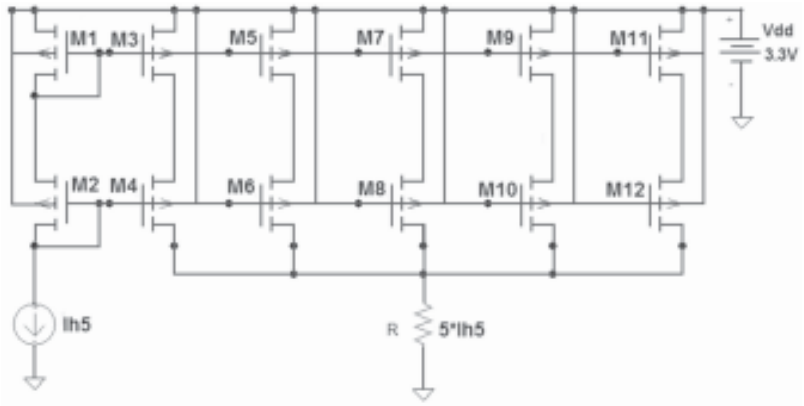


Figure 4- Scaler circuit h5 based on cascode current mirror.

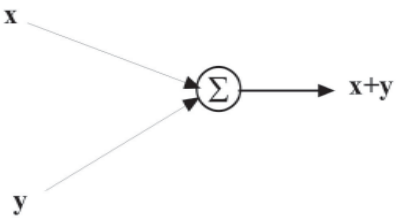


Figure 5- Block diagram of adder circuit.

2.3 Multiplier - Divider Circuit

The multiplier-divider circuit is used to determine the output of the defuzzifier circuit. It is analogous to that proposed by (Martin, 2001), that is based on MOS translinear principle operating in saturation mode. This circuit is employed to multiply the position of membership function determined in 5μA, by the sum of scaled activation degree ($\sum f^*$), and to divide this result by the sum of activation degree ($\sum f$) (Equation (3)).

The multiplier-divider circuit is implemented using a geometric mean circuit and a squarer-divider circuit, as shown in Fig. 6.

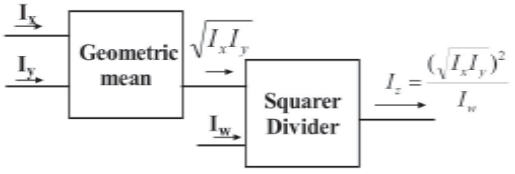


Figure 6- Principle of multiplier-divider circuit.

$$I_{out} = \frac{I_x * I_y}{I_w} = \frac{\left(\sqrt{I_x * I_y}\right)}{I_w} \qquad (4)$$

The geometric mean and squarer-divider circuits are based on the voltage translinear loop. The voltage translinear loop in up-down topology is formed of four type N MOS transistor with same dimensions, in saturation mode (Fig. 7).

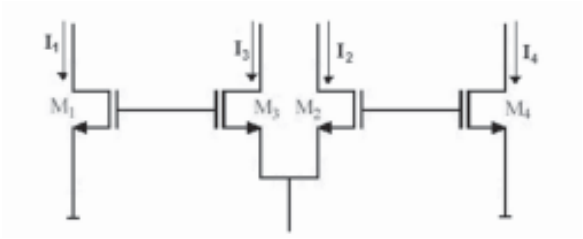


Figure 7- Voltage translinear loop in up-down topology.

The equation of this translinear circuit is:

$$V_{gs_1} + V_{gs_2} = V_{gs_3} + V_{gs_4}. \qquad (5)$$

The voltage between gate and source, V_{gs} ,in saturation mode, is:

$$V_{gs} = V_{th} + \sqrt{\frac{I}{k\frac{W}{L}}} \qquad (6)$$

Where I is the drain current, V_{th} is the threshold voltage, W is the channel width and L is the channel length. From Equation (5) and (6), the equation that relates the currents in the circuit is obtained.

Squaring both sides in Equation (7), the following expression is obtained:

$$2\sqrt{I_1 I_2} + I_1 + I_2 = 2\sqrt{I_3 I_4} + I_3 + I_4. \qquad (8)$$

For $I_3 = I_4$ and $I_z = \sqrt{I_1 I_2}$, then:

$$I_3 = I_4 = \frac{2I_z + I_1 + I_2}{4}. \qquad (9)$$

Geometric Mean Circuit. The geometric-mean circuit (Fig. 8) can be readily obtained from up-down loop of Fig. 7, by setting the input and output currents.

The type P MOS current mirror circuit is used to inject a proper current in voltage translinear loop. In this circuit the cascode current mirror was employed to reduce the mirroring error.

$$I_1 = I_x, \quad I_2 = I_y \quad \text{e} \quad I_3 = I_4 = \frac{2I_z + I_x + I_y}{4}. \qquad (10)$$

$$I_z = \sqrt{I_x I_y} \qquad (11)$$

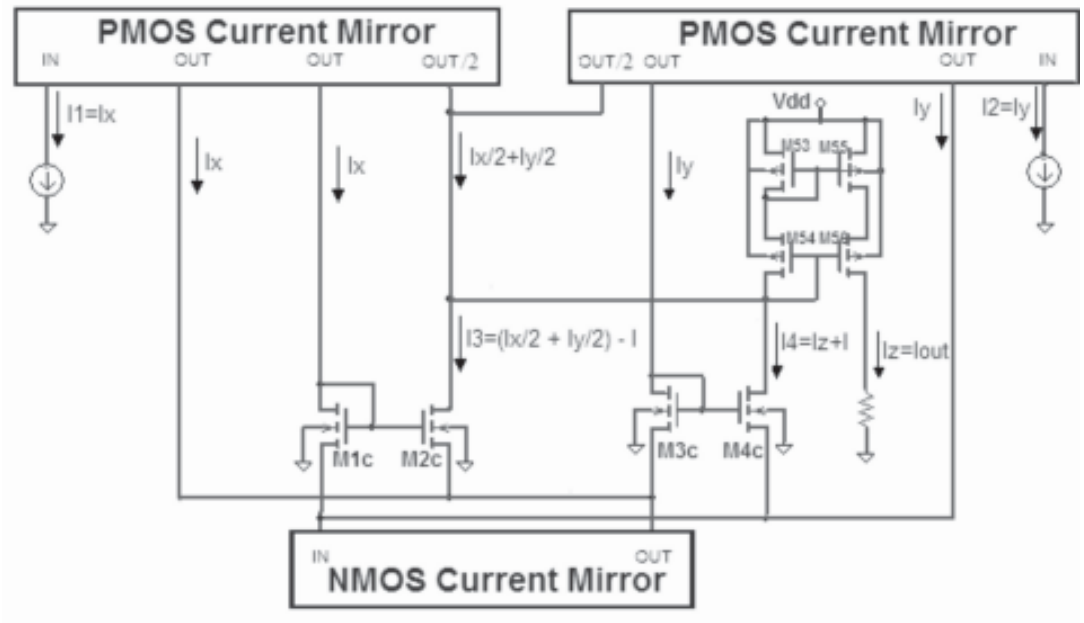


Figure 8- Geometric-mean circuit schematic.

Squarer - Divider Circuit. The squarer-divider circuit (Fig. 9) is obtained by performing a minor change on the geometric-mean circuit of Fig. 8, in order to transform its geometric-mean output into a low-impedance squarer-divider input, and one of its low-impedance inputs into the high-impedance squarer-divider output.

The squarer-divider output current is obviously given by the inverse of Equation (11):

$$I_{out} = \frac{I_z^2}{I_w} \qquad (12)$$

Multiplier - Divider Circuit. The multiplier-divider circuit (Fig. 10) is obtained when the output of the geometric mean circuit of Fig. 8 is injected in the input of the squarer-divider circuit of Fig. 9, through a type N MOS cascode current mirror.

3. Results

Circuits were simulated using the SPICE and CMOS 0.35 m technology models supplied by AMS, with 3.3V power supply voltage. To verify the function of the geometric-mean circuit, the triangular wave and direct current, shown in the upper part of Fig. 11, were used

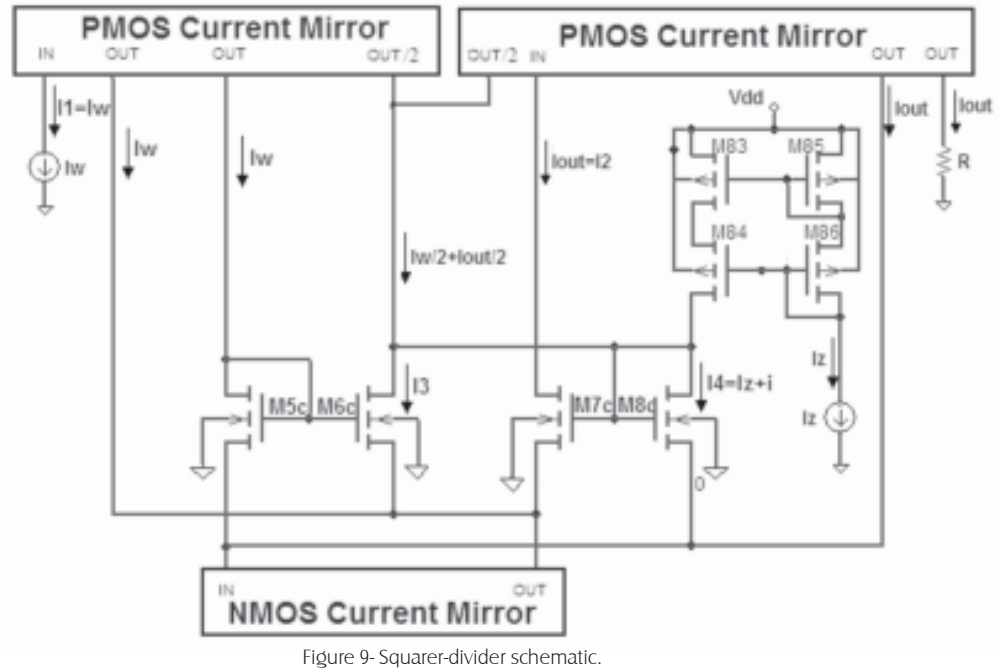


Figure 9- Squarer-divider schematic.

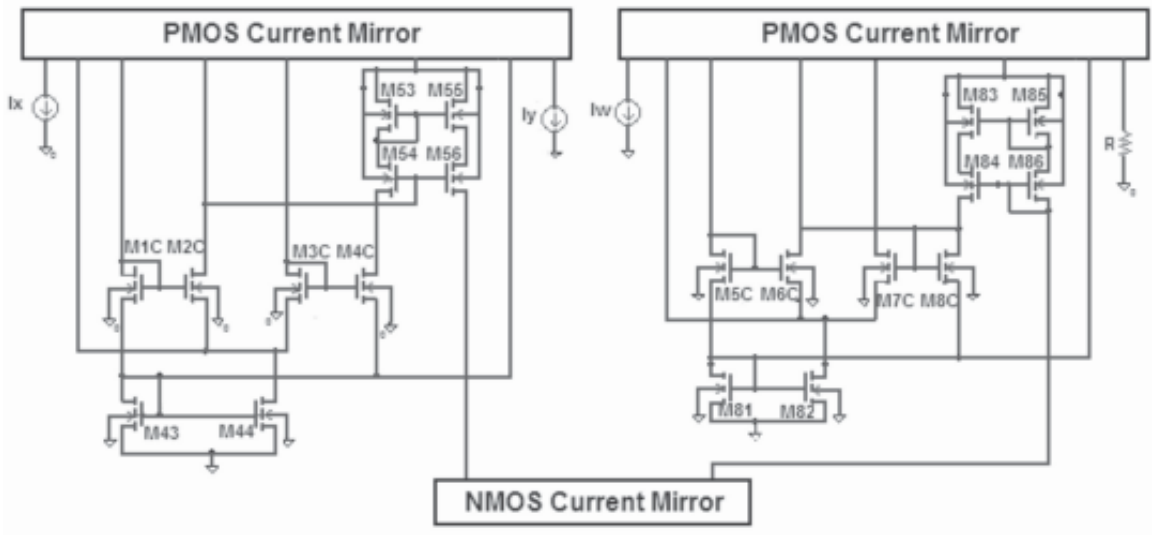


Figure 10- Multiplier-Divider circuit.

as its input currents, Ix and Iy, respectively. The lower part of Fig. 11 shows the ideal output current and the output current of this circuit, for which the error is less than 0.4% of full scale. Also the dynamic range (defined as the maximum range in which the error of the circuit is acceptable) is:

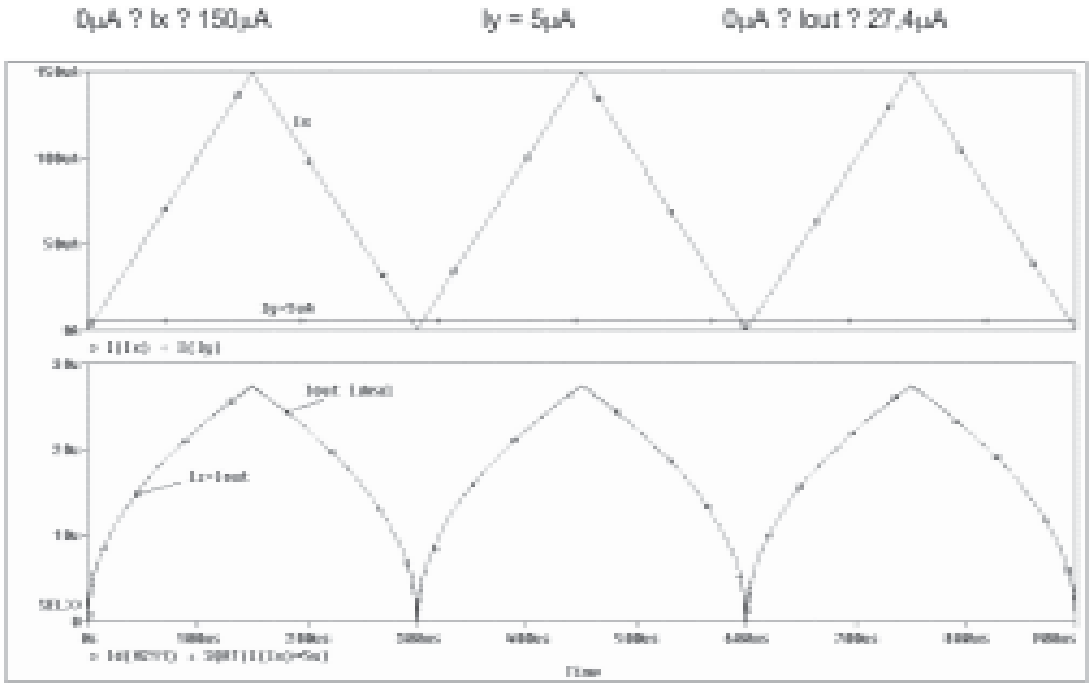


Figure 11- Simulation results for the geometric-mean circuit.

Similarly, the triangular-wave and direct current were applied to the squarer-divider circuit as its input, Iz and Iw, respectively. The simulation results are illustrated in Fig. 12.

The upper part of this figure shows the input currents, and the lower part is the output current, for which the error is less than 1.5% of full scale. The dynamic range of this circuit is:

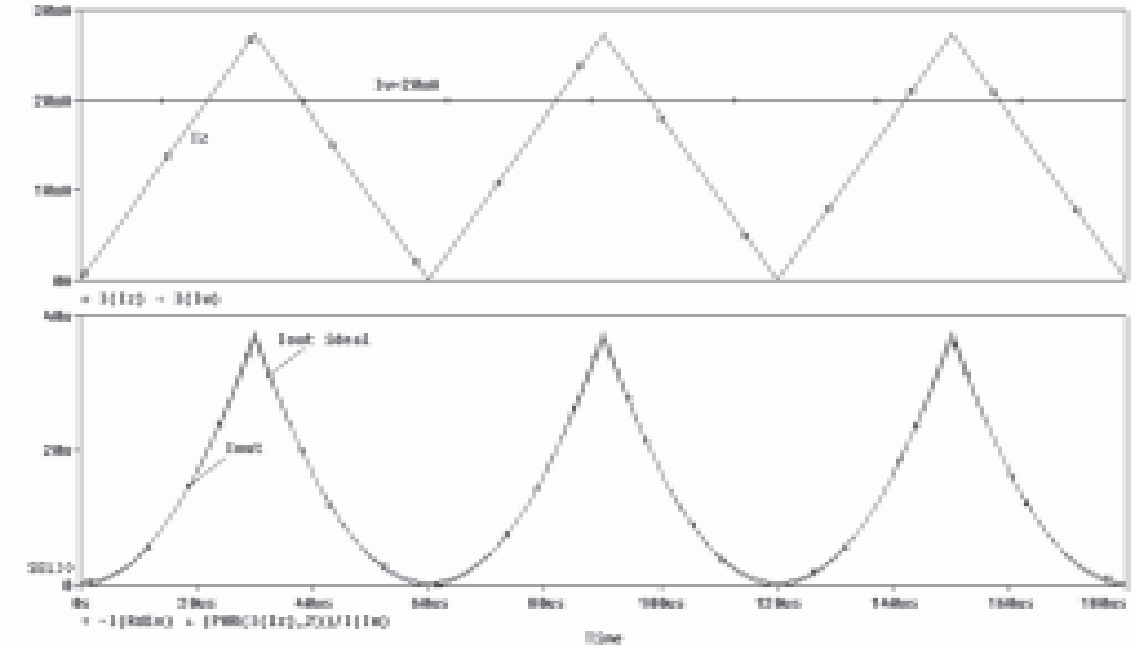


Figure 12- Simulation results for the squarer-divider circuit.

0μA ? Iz ? 27,38μA

10μA ? Iw ? 50μA 0μA ? Iout ? 75μA

To verify the function of the first quadrant multiplier-divider circuit, the triangular wave Ix and direct currents with Iy=5 A and Iw=10 A were used as its input currents, shown in the upper part of Fig. 13. The lower part of the Fig. 13 is the output current compared with the ideal output current for which the error is less than 1.8% of full scale.

Based on the value of the sum of the scaled activation degree ($\sum f^*$) and the sum of activation degree ($\sum f$), of the Equation (3). The DC transfer characteristics of the presented multiplier-divider, shown in Fig. 14, indicate high linearity within the ranges shown in Table 1.

The simulation result of the defuzzifier circuit is shown in Fig. 15. The inputs of Height defuzzifier circuit is composed of activation degrees currents I_{h1}, I_{h2}, I_{h3}, I_{h4} e $I_{h5} \in$ [0μA, 10μA]. The currents signal in the middle part of the Fig. 15 are the sum of the scaled activation degree current ($I \sum f^* = Ix$), which is the output of the

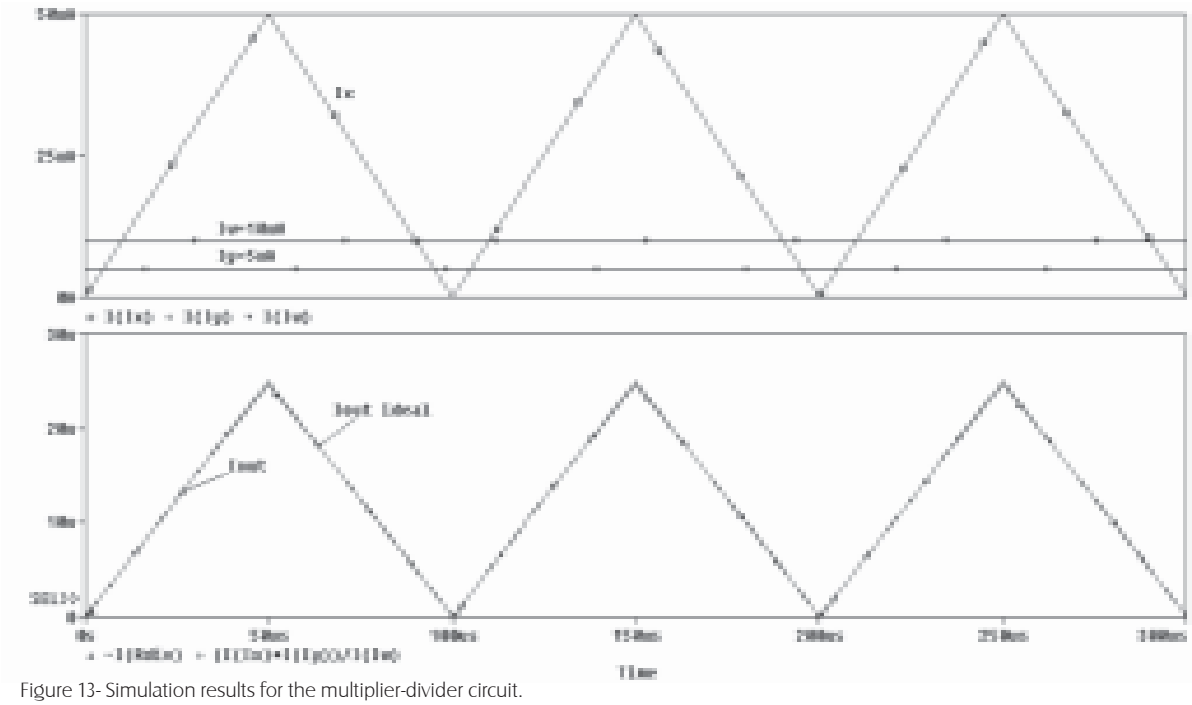


Figure 13- Simulation results for the multiplier-divider circuit.

scaler circuit (Fig. 3) and the error is less than 0.2% of full-scale range. And also, the sum of activation degree current ($I \sum f = Iw$) and the current Iy=5μA. The lower part of Fig. 15 is the defuzzifier output current Iout and ideal output current. It is apparent that this circuit can perform the function of Height defuzzifier circuit. The error in this simulation is less than 2% of full scale range.

Table 1. Linearity ranges of the multiplier-divider circuir

Iy	Iw	Ix	Iout
5μA	5μA	5μA ? Ix?25μA	5μA ? Iout ? 25μA
5μA	10μA	10μA ? Ix?50μA	5μA ? Iout ? 25μA
5μA	20μA	30μA ? Ix? 90μA	7,5μA ? Iout ? 22,5μA
5μA	30μA	60μA ? Ix? 120μA	10μA ? Iout ? 20μA
5μA	40μA	100μA <= Ix<= 140μA	12,5μA ? Iout ? 17,5μA
5μA	50μA	Ix= 150μA	Iout = 15μA

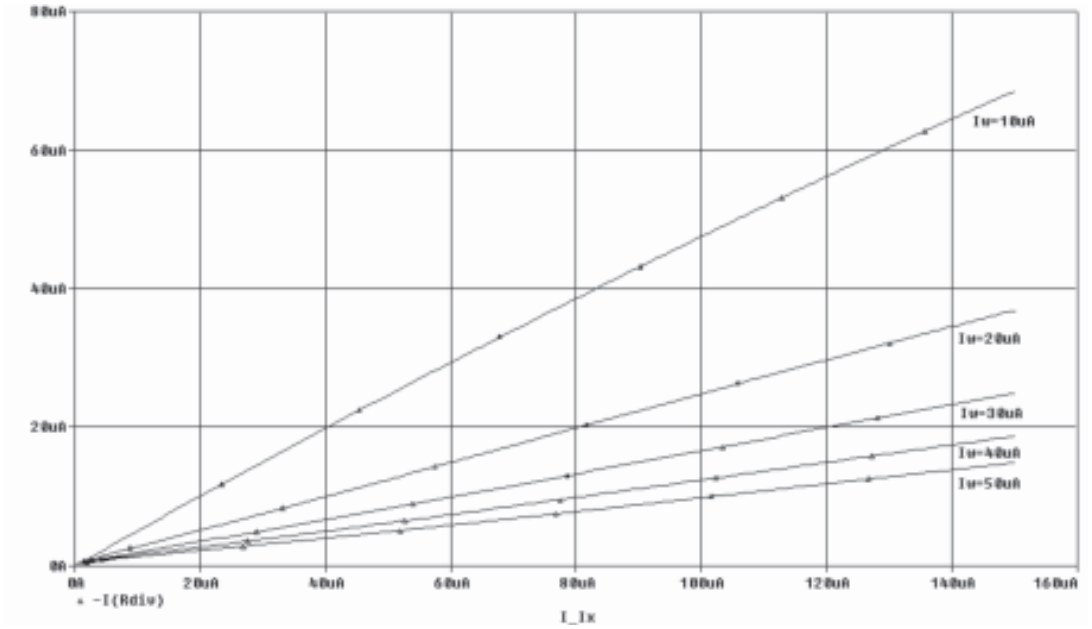


Figure 14- Simulation of DC Characteristic of the multiplier-divider circuit.

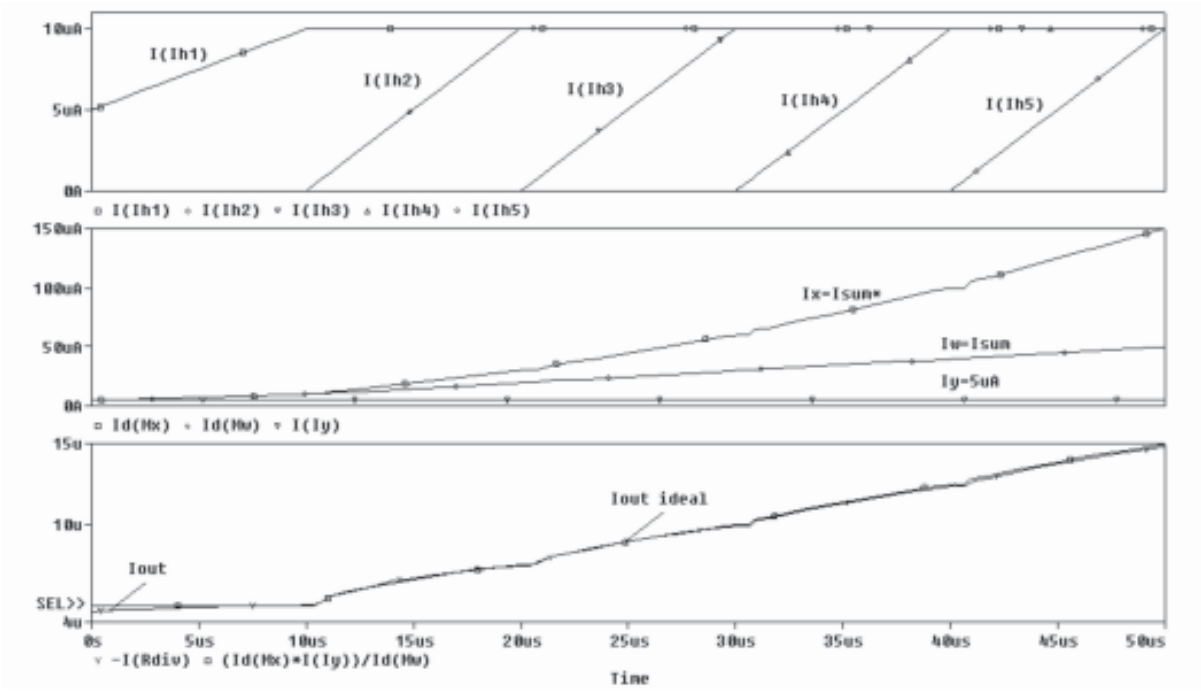


Figure 15- Simulation results for defuzzifier circuit.

4. Conclusions

Efficient solutions at architectural and operator level have been provided to implement the current-mode Height defuzzifier circuit. The functional blocks of this circuit has been presented in this paper: the scaler circuit, the adder circuit and the divider circuit to obtain the control output. The mathematical operations required in the different function blocks are easy implemented with current-mode techniques, and thus result in very simple circuits. This circuit has been simulated using the SPICE and CMOS 0.35μm technology models supplied by AMS. The simulated results indicated that the proposed circuit can work

well. In addition, to the function testing and its transient response were also tested. The proposed defuzzifier circuit can be used as part of a fuzzy microprocessor, and can be applied to many control systems, as for exempla in industrial applications that use fuzzy control.

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